WHAT IS CLAIMED IS:

1. Device for the correction of the power factor in power supply units with forced switching operating in transition mode, comprising a converter and a control device coupled to said converter so as to obtain network alternating input voltage and regulated voltage on the output terminal, said converter comprising a power transistor, said control device comprising a pilot circuit suitable for determining the switched-on time and switched-off time of said power transistor, characterised in that said control device comprises control means coupled to said pilot circuit and with said converter and capable of prolonging said period of switched-on time of the power transistor at the instants of time in which said alternating main voltage assumes a value that is substantially zero.

2. Device according to claim 1, characterized in that said converter comprises a rectifier circuit of said network input voltage, said control device comprises an error amplifier having a first signal on the inverting input that is proportionate to said regulated voltage and a reference signal on the non-inverting terminal, and said pilot device comprises a multiplier having a second signal at the input that is proportionate to the voltage rectified by said rectifier circuit and an error signal at the output from said error amplifier, a comparator that is suitable for comparing a third signal at the output from said multiplier and a fourth signal proportionate to the current that flows through said power transistor, a fifth signal at the output from said comparator being suitable for determining the period of switched-on time and of switched-off time of said power transistor, said control means being suitable for increasing the value of one of the said third and fourth signals at the comparator input at the time instants wherein the network voltage has a value that is substantially zero.

3. Device according to claim 2, characterized in that said control means comprises a circuit means capable of adding a negative voltage offset to said fourth signal.

4. Device according to claim 3, characterized in that said converter comprises an inductor arranged between a non-pilotable terminal of said power transistor and said rectifier circuit and said device for the correction of the power factor comprises an auxiliary coil of said inductor, said circuit means being

connected to said auxiliary coil and to the output of said error amplifier and determining said voltage offset during the period of switched-on time of said power transistor when the voltage signal at the heads of said auxiliary coil assumes a negative value.

5. Device according to claim 4, characterized in that said circuit means comprise a diode having a cathode connected to said auxiliary coil and the anode connected to a terminal of a capacitor the other terminal be earthed to a terminal of a first resistance the other terminal being connected to the input of the comparator on which said fourth signal is present, a second resistance arranged between the output of said error amplifier and the input of the comparator on which said fourth signal is present.

6. Device according to claim 5, characterized in that said circuit means comprise a third resistance on a terminal of which said second signal persists and the other terminal being connected to the input of the comparator on which said fourth signal is present.

7. Device according to claim 2, characterized in that said control means comprises a circuit capable of adding a portion of either the second signal or the error signal to the third signal leaving said multiplier.

8. Device according to claim 7, characterized in that either the second signal or the error signal is subtracted from a constant level signal and is multiplied by a constant to obtain said signal portion to add to the third signal.

9. Device according to claim 2, characterized in that said control means comprises a circuit capable of adding a first portion of the second signal and a second portion of the error signal to the third signal leaving said multiplier.

10. Device according to claim 9, characterized in that the second signal and the error signal are subtracted from constant level signals and are multiplied by a constant to obtain said first and second signal portion to add to said third signal.

11. Device according to claim 2, characterized in that said control means comprises a circuit capable of adding a portion of the error signal to the third signal at the output from said multiplier when said second signal is below a set value.

12. Device according to claim 11, characterized in that the error signal is subtracted from a constant level signal and is multiplied by a constant to obtain said signal portion to add to said third signal only if said second signal is lower than said set value.

13. Device according to claim 12, characterized in that said set value is said signal portion multiplied by a constant.

14. Device according to claim 7, characterized in that said control means can be integrated into a chip with the pilot circuit of said control device.

15. A controller for regulating an output signal that a boost converter generates from a time-varying input signal, the boost converter having a power switch and the input signal having a crossover amplitude, the controller comprising:

an error circuit operable to periodically activate the power switch for an on period that is related to the input and output signals; and

a distortion-reducing circuit coupled to the error circuit and operable to lengthen the on period while the input signal is within a predetermined amplitude range.

16. The controller of claim 15 wherein the error circuit comprises:

an amplifier operable to generate an error signal that is related to the output signal;

a multiplier operable to generate a product of the error signal and a first signal derived from the input signal; and

a comparator operable to activate the power switch while a second signal derived from a current through the switch is less than the product.

17. The controller of claim 15 wherein:

the error circuit comprises:

an amplifier operable to generate an error signal that is related to the output signal,

a multiplier operable to generate a product of the error signal and a first signal derived from the input signal, and

a comparator operable to activate the power switch while a second signal derived from a current through the switch is less than the product;

the distortion-reducing circuit is operable to add an offset signal to the second signal while the input signal is within the predetermined amplitude range;

the on period begins substantially when the current through the switch equals zero; and

the on period ends substantially when a sum of the second signal and the offset signal equals the product of the error voltage and the first signal.

18. The controller of claim 15 wherein the predetermined amplitude range includes the crossover amplitude.

19. The controller of claim 15 wherein the predetermined amplitude range is substantially centered about the crossover amplitude.

20. A power supply, comprising:

a boost converter having a power switch and operable to generate an output voltage from a time-varying input voltage signal; and

a controller coupled to the converter and including,

an error circuit operable to periodically activate the power switch for an on period that is related to the input voltage signal and the output voltage; and

a distortion-reducing circuit coupled to the error circuit and operable to lengthen the on period while the input voltage signal is within a predetermined voltage range.

21. The power supply of claim 20 wherein the input voltage signal comprises a sinusoidal voltage signal.

22. An electronic system, comprising:

a power supply that includes,

a boost converter having a power switch and operable to generate an output voltage from a time-varying input voltage signal, and

a controller coupled to the converter and including,

an error circuit operable to periodically activate the power switch for an on period that is related to the input voltage signal and the output voltage; and

a distortion-reducing circuit coupled to the error circuit and operable to lengthen the on period while the input voltage signal is within a predetermined voltage range.

23. A method, comprising:

generating an output signal from a time-varying input signal;

regulating the output signal by periodically drawing current through an inductor for an on period that is related to the input and output signals; and

lengthening the on period while the input signal is within a predetermined amplitude range.

24. The method of claim 23 wherein lengthening the on period comprises lengthening the on period while the input signal is within a predetermined amplitude range that includes zero amplitude.

25. The method of claim 23 wherein lengthening the on period comprises periodically drawing the current through the inductor by closing a switch for the on period.

26. The method of claim 23 wherein:

the output signal comprises a substantially DC voltage signal;

the input signal comprises a sinusoidal voltage signal; and

the predetermined amplitude range comprises a predetermined voltage range.

27. The method of claim 23 wherein:

regulating the output signal comprises,

generating an error signal by comparing the output signal to a reference signal,

generating a comparison product by multiplying the error signal by the input signal,

comparing the comparison product with a comparison signal that represents the current drawn through the inductor during the on period, and

ceasing drawing current through the inductor when the comparison signal equals or exceeds the comparison product; and

lengthening the on period comprises adding an offset signal to the comparison signal.

28. The method of claim 27, further comprising generating the offset signal in relation to the current through the inductor.

29. The method of claim 27, further comprising generating the offset signal in relation to the input signal.

30. The method of claim 27, further comprising generating the offset signal in relation to the error signal.

31. The method of claim 27, further comprising generating the offset signal in relation to the comparison signal.